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(54) Title: PROCESS FOR MAKING A PARYLENE COATING

(57) Abstract

Multi-level structures including a first layer with a parylene polymer layer deposited thereon as well as methods of making the same. The parylene polymer layers can exhibit enhanced properties such as adhesion and/or strength. The parylene polymer layers can have relatively low levels of impurities. In certain embodiments, the parylene polymer layers are formed using a pulsed plasma treatment.

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PROCESS FOR MAKING A PARYLENE COATING

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CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

The present application is a continuation application under 35 U.S.C. §120 of U.S. Patent Application Serial No. 08/791,609, entitled Parylene Polymer Layers, and filed January 31, 1997, which is a continuation application under 35 U.S.C. §120 of U.S. Patent Application Serial No. 08/738,319, entitled Parylene Polymer Layers, and filed October 25, 1996.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to improved parylene polymer layers, methods of making the same and methods of using the same.

2. Discussion Of The Related Art

Semiconductors are widely used in integrated circuits for electronic products systems such as computers and televisions. These integrated circuits typically combine many transistors on a single crystal silicon chip to perform complex functions and store data. Semiconductor and electronics manufacturers, as well as end users, desire integrated circuits which can accomplish more in less time in a smaller package while consuming less power. However, some of these desires may be in opposition to each other. For example, simply shrinking the feature sizes on a given circuit from 0.5 microns to 0.25 microns can increase power consumption by 30%. Likewise, doubling operational speed generally doubles power consumption. Miniaturization also generally results in increased capacitive coupling, or cross talk, between conductors which carry signals across the chip. This can limit achievable speed and degrade the noise margin used to insure proper device operation.

One way to diminish power consumption and cross talk effects is to decrease the dielectric constant of electrically insulating layers that separate layers of electrically conductive materials within the integrated circuit. In addition, since operational conditions may include high temperatures, it can be advantageous to use materials with relatively high thermal stability to form the insulating layers.

Silicon dioxide is one of the most common materials used in insulating layers for integrated circuits. However, silicon dioxide is non-ideal due to its comparatively high dielectric constant of about 3.9.

Layers formed from parylene polymers have been proposed for use as insulating layers in integrated circuits because these materials have relatively low dielectric constants and comparatively high melting temperatures. Parylene polymers are poly-p-xylylenes which may be prepared starting with a dimer having the structure:

$$\begin{array}{c} C \times_2 - C \times_2 \\ O & O \\ C \times_2 - C \times_2 \end{array}$$

wherein X is typically a hydrogen or a halogen. The most common forms of parylene dimers

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Polymer films formed from these parylene dimers may have comparatively low dielectric constants and relatively high melting temperatures. However, these parylene polymer films have relatively high dielectric constants and inferior thermal stabilities, rendering them less attractive for use in integrated circuits.

Typically, a vapor deposition method is used to form parylene polymer layers from parylene dimers. One such vapor deposition method is disclosed in *Journal of Applied Polymer Science* 13, 2325 (1969). According to this method, commonly referred to as the Gorham process, the parylene dimer is cracked at an elevated temperature to produce parylene monomer having the structure:

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The parylene monomer is condensed onto a substrate at a temperature of from about room temperature to about -35°C. Under these conditions, the parylene monomer simultaneously polymerizes on the substrate to form a layer of the parylene polymer adhered to the substrate.

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A vapor deposition process for forming poly-p-xylylene films from other than parylene dimer materials is disclosed in U.S. Patent No. 5,268,202 (You). The method disclosed by this reference includes forming the monomer vapor inside the vacuum chamber in which deposition occurs, precluding the purification opportunities afforded by the parylene dimer process prior to deposition on the substrate. Therefore, the resulting poly-p-xylylene layers have relatively high impurity levels. For example, *Journal of Vacuum Science and Technology* A11(6), 3057 (1993) discloses that poly-p-xylylene films formed by the method of You have zinc impurity levels of about 3%. Such a comparatively high level of zinc impurity results in problems with the poly-p-xylylene film relating to, for example, increased dielectric constant, decreased surface resistivity, ion movement within the layer, film surface charging effects and/or electron storm formation when the poly-p-xylylene film is used within a multi-level structure. As a result, these poly-p-xylylene films cannot be used in integrated circuits.

Combining the use of a plasma with the deposition of a gaseous species has been used in many systems. For example, DUMIC Conference, February 11, 1997, ISMIC-222D/97/0098-105 (hereinafter "DUMIC") discloses the use of a pulsed plasma to manipulate the control of fluorocarbon thin films on silicon. This reference focuses on controlling the relative amounts of CF₃, CF₂ and CF, rather than any effects on the deposition rate, deposition efficiency or adhesion of the resulting surface. Furthermore, DUMIC does not disclose the use of a pulsed plasma in conjunction with the formation of a parylene polymer film. As known to those skilled in the art, variation in the parameters used in connection with a pulsed plasma (e.g., peak power amplitude, peak power frequency and duty cycle) is dependent upon the surface created during deposition.

Hence, it remains a challenge in the art to provide an electrically insulating layer for use in integrated circuits of electronic devices that has a relatively low dielectric constant and comparatively high melting temperature. It is a further challenge in the art to provide such an

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insulating layer which is formed from a parylene polymer.

SUMMARY OF THE INVENTION

In its broadest aspects, the present invention relates to improved parylene polymer layer, methods of making these layers and methods of using these layers. In one aspect, the improved parylene polymer layers have relatively low levels of impurities such as, for example, zinc. In another aspect, the improved parylene polymer layers are formed by the use of a pulsed plasma treatment. In a further aspect, the improved parylene polymers have other chemical species incorporated therein. In still a further aspect, different combinations of the aforementioned aspects are combined to improved provide parylene polymer layers that have relatively low levels of impurities, that are formed using a pulsed plasma treatment and/or that have other chemical species incorporated therein.

In one illustrative embodiment, the present invention provides a method of forming a parylene polymer layer. The method comprises depositing monomers of parylene onto the surface of a substrate to form a layer, and treating the layer with a pulsed plasma treatment.

In another illustrative embodiment, the present invention provides a multi-level structure. The structure comprises a first layer, a parylene polymer layer and a layer of adhesion promotion material. The parylene polymer layer is disposed along the first layer, and the layer of adhesion promotion material is disposed along the layer of adhesion promotion material. The parylene polymer layer is formed form a material that has a structure:

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wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at

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most about 66 parts per billion.

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In yet another illustrative embodiment, the present invention provides a method making a multi-level structure. The method comprises depositing a monomer on the surface of a substrate to form a layer, and treating the layer with a pulsed plasma treatment to form a parylene polymer film on the surface of the first layer. The parylene polymer has a structure:

wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 66 parts per billion.

In a further illustrative embodiment, the present invention provides a multi-level structure. The structure comprises a first layer and a parylene polymer layer disposed along the surface of the first layer. The parylene polymer layer is formed from a material having a structure:

wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero, and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 66 parts per billion. The parylene polymer layer is formed by a process including the

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steps of: depositing monomers of parylene onto a surface of a substrate to form a layer; and treating the layer with a pulsed plasma treatment.

In still a further illustrative embodiment, the present invention provides a multi-level structure. The structure comprises a first layer and a parylene polymer layer disposed along the surface of the first layer. The parylene polymer is formed by a process including the steps of: depositing monomers of parylene onto a surface of a substrate to form a layer; and treating the layer with a pulsed plasma treatment.

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BRIEF DESCRIPTION OF THE DRAWINGS

The advantages and features of the present invention will be more clearly understood in view of the following detailed description when taken in conjunction with the drawings, in which:

Fig. 1 is a cross-sectional view of one embodiment of a multi-level structure according to the present invention;

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- Fig. 2 is a cross-sectional view of another embodiment of a multi-level structure according to the present invention;
- Fig. 3 is a block diagram of one embodiment of a vacuum deposition system which may be used to form parylene polymer layers according to the present invention;
- Fig. 4 is a cross-sectional view of a portion of one embodiment of an integrated circuit including a multi-level structure according to the present invention; and
- Fig. 5 is a block diagram of one embodiment of a vacuum chamber which may be used to form parylene polymer layers according to the present invention.

DETAILED DESCRIPTION

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Fig. 1 depicts a multi-level structure 10 according to the present invention. Structure 10 includes substrate layer 12 and parylene polymer layer 14. By "parylene polymer" it is herein meant to refer to a poly-p-xylylene. Typically, a parylene polymer is formed from a parylene dimer.

Substrate layer 12 may be formed from any materials onto which parylene polymer layer 14 is capable of being deposited. These materials may include electrically conductive and electrically

non-conductive materials. The particular material from which layer 12 is formed depends upon the application, and such materials are known to those skilled in the art. For example, substrate layer 12 may be formed from organic materials or inorganic materials including, but not limited to, aluminum, iron, steel, molybdenum, aluminum oxide, titanium oxide, lead oxide, copper oxide, iron oxide, beryllium oxide, manganese oxide, tungsten oxide, tantalum oxide, vanadium oxide, silicones, natural rubbers, plastics, plastic composites, cellulosic materials, epoxy-containing compounds, thermosetting compounds, thermoplastic compounds, oxides of silicon (e.g., fly ash, hydrated silica, silica, quartz, aerogels, xerogels and fumed silica) and the like. Furthermore, layer 12 may comprise gallium arsenide or other binary semiconductors.

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Substrate layer 12 may also be formed from a vacuum compatible liquid. By "vacuum compatible" it is herein meant to refer to a material that has a vapor pressure at the operating temperature of the vacuum chamber used such that the minimum pressure to which the vacuum chamber can be pumped is independent of the presence of the vacuum compatible material. One example of a vacuum compatible liquid is gamma-methacryloxypropyltrimethoxysilane.

In certain embodiments, substrate layer 12 may be a printed circuit board, a silicon backboard, a fiberglass backboard, a silicon wafer, paper, a key pad, a catheter, a pacemaker cover, a subcutaneous probe, a bird feather, a silicone O-ring, parts of a mechanical apparatus, such as an automobile, or the like.

Parylene polymer layer 14 is formed from a material having the structure:

m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, an alkyl group, a cyclo hydrocarbon an, alkylene group or an alkylyne group having the general formula $C_nH_\nu X_{\nu\nu}$, wherein X is a halogen, n is an integer greater than zero and z is 1. If G is an alkyl group

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(i.e., saturated) then y + w = 2n+1. If G is a cyclo hydrocarbon, an alkylene or alkylyne group (i.e., G has at least one degree of unsaturation) then y + w is less than 2n+1 by a factor of twice the degree of unsaturation.

Fig. 2 depicts another multi-level structure 20 according to the present invention. Structure 20 includes parylene polymer layer 14 disposed between a first layer of material 16 and a second layer of material 18. Although not limited to these materials, layers 16 and 18 may be formed from any of the materials listed above with reference to substrate layer 12. Furthermore, layer 16 and/or layer 18 may take on any of the above-noted shapes of substrate layer 12. Layer 16 and/or layer 18 may take on other shapes as well.

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In certain embodiments, each of layers 16 and 18 may be formed from materials that are at least partially electrically conductive. In such embodiments, layers 16 and 18 may be formed from metals using standard photolithographic and etching techniques. For these embodiments, layers 16 and 18 may each correspond to a power plane, a ground plane or a metal interconnection trace layer. Other processes for forming layers 16 and 18 are known to those skilled in the art and are intended to be within the scope of the present invention.

In some embodiments, parylene polymer layer 14 may be relatively difficult to adhere to certain other materials. For these embodiments, it may be desirable to promote the adhesion of layer 14 to other surfaces. Accordingly, parylene polymer layer 14 may undergo certain surface treatments to increase its ability to adhere to other surfaces. Such treatments include, for example, continuous plasma treatment (i.e., substantially 100% duty cycle), corona treatment, charge treatment and/or other surface roughening treatments. These treatments are known to those skilled in the art and are intended to be within the scope of the present invention. For example, in a continuous plasma treatment, a radio frequency (RF) generator can be used in conjunction with a background pressure of one or more gases to produce a plasma.

During parylene monomer deposition, a pulsed plasma treatment has been found to increase the adhesion of the parylene monomer. By "pulsed plasma treatment" it is herein meant to refer to a plasma treatment in which the duty cycle (i.e., the percentage of time that the plasma is on during the treatment) is less than about 100%. Typically, the duty cycle of a pulsed plasma treatment is at most about 50%. Preferably, the duty cycle of a pulsed plasma treatment is from about 0.1% to

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about 50%, more preferably from about 0.1% to about 10% and most preferably about 0.2%.

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Fig. 3 shows a block diagram of one embodiment of a vacuum system 80 having a pulsed plasma source appropriate for use in forming parylene polymer layers according to the present invention. System 80 includes a parylene monomer source 82, a deposition chamber 84, a substrate 86, and a platen 88 (see discussion below). In addition, system 80 includes a pulsed plasma source 90 connected to chamber 84 to allow a parylene polymer layer disposed on substrate 86 to undergo a pulsed plasma treatment. Pulsed plasma source 90 includes an RF generator 92 (model 300-1 RF generator, available from Technics Company, located in Alexandria, VA). A timing module 93 (model DMP10-.1-.4, available from Dynatronics, Inc., located in Amery, WI) interfaces pulsed plasma source 92 to a timing circuit 94 to control the duty cycle of the pulsed plasma treatment. Such timing circuits 94 are known to those skilled in the art. Furthermore, while particular examples of an RF generator and a timing module are disclosed herein, other such devices are known to those skilled in the art and are intended to be within the scope of the present invention.

During a pulsed plasma treatment, a background pressure of parylene monomer (e.g., from about 10 to about 15 millitorr) is present in chamber 82. As the parylene monomer is deposited on the surface of substrate 86, a pulsed plasma treatment occurs such. For example, if the duty cycle of the pulsed plasma is about 0.2%, the RF generator is on about 0.2% of the time that the parylene monomer is being deposited on the surface of substrate 86. Within the plasma, various ions, radicals and other species are formed from the parylene monomer gas. These species generally have high sticking coefficients and deposit on the surface of substrate 86 with high efficiency, resulting in a parylene polymer layer having enhanced properties as described herein.

The peak power of RF generator 92 during a pulsed plasma treatment can be varied depending upon the desired properties of the resulting parylene polymer layer. Generally, this peak power depends upon the volume of the deposition chamber, with the peak power increasing as the volume of the deposition chamber increases. If the peak power of generator 92 is too low, the pulsed plasma treatment may have minimal effect on improving the properties of a parylene polymer layer. However, if the peak power of generator 92 is too high, the resulting parylene polymer layer may be brittle, nontransparent or otherwise have undesirable properties. Accordingly, the peak power of RF generator 92 during a pulsed plasma treatment relative to the volume of the deposition

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chamber is preferably from about 0.05 Watts/inch³ to about 100 Watts/inch³, more preferably from about 0.1 Watts/inch³ to about 20 Watts/inch³ and most preferably from about 0.1 Watts/inch³ to about 10 Watts/inch³.

The increased adhesion associated with using a pulsed plasma treatment during parylene monomer deposition results in an increased thickness of the resulting parylene polymer film and an increased rate of deposition of the parylene monomer.

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While holding other variables constant, relative to a parylene polymer film formed without a pulsed plasma treatment, a parylene polymer layer formed using a pulsed plasma treatment is preferably at least about 1.5 times as thick, more preferably at least about 2 times as thick and most preferably at least about 3 times as thick.

While holding other variables constant, relative to a parylene polymer film formed without a pulsed plasma treatment, the deposition rate of parylene monomer using a pulsed plasma treatment is preferably at least about 1.5 fast, more preferably at least 2 times as fast and most preferably at least 3 times as fast.

Surprisingly, in addition to providing enhanced adhesion, it has been found that treating the surface of a parylene polymer layer using a pulsed plasma results in other advantages. One such advantage relates to improved control over the surface onto which the parylene polymer layer is formed. Usually, when forming a parylene polymer layer on a substrate for use in the electronics industry, it is desirable to leave an area of about 1 mm thickness around the edge of the substrate that is substantially free of parylene polymer. This concept is commonly referred to within the art as edge exclusion. In addition, it is advantageous to minimize the amount of parylene polymer that forms on the underside of a substrate (i.e., on the side that is not directly facing the parylene monomer gas). Problems with accomplishing these goals can occur as a result of the deposition process in which the substrate is typically clamped to a platen at only a select few locations (e.g., 6 locations), such as described in commonly assigned U.S. Patent No. 5,546,473, which is herein incorporated by reference. Surprisingly, it has been found that enhanced edge exclusion and reduced parylene polymer formation on the underside of the substrate are achieved when a parylene polymer layer undergoes pulsed plasma treatment relative to parylene polymer layers that undergo no plasma treatment or continuous plasma treatment.

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An additional advantage to using a pulsed plasma treatment when forming a parylene polymer layer relates to the dielectric constant of the resulting parylene polymer layer. In many embodiments, such as when the parylene polymer layer is used as an insulating layer, such as in the electronics industry, it is advantageous for the parylene polymer layer to have a minimal dielectric constant. Furthermore, it is often desirable that the in-plane dielectric constant (i.e., the dielectric constant parallel to a plane of the substrate) and out-of-plane dielectric constant (i.c., the dielectric constant in a plane perpendicular to the substrate) of the parylene polymer layer be approximately equal. Unexpectedly, it has been found that pulsed plasma treatment of a parylene polymer layer results in a parylene polymer layer with reduced dielectric constants relative to the dielectric constants of parylene polymer layers formed with no plasma treatment or with a continuous plasma treatment, and, surprisingly, the values of the in-plane dielectric constants and out-of-plane dielectric constants of parylene polymer layers formed using pulsed plasma treatment are closer to the same than the values of the in-plane and out-of-plane dielectric constants for parylene polymer layers formed with no plasma treatment or with a continuous plasma treatment. Hence, relative to a parylene polymer layer formed without using a pulsed plasma treatment, a parylene polymer layer formed using a pulsed plasma treatment can have a reduced dielectric constant and/or a dielectric constant that is more isotropic.

Pulsed plasma treatment or continuous plasma treatment of a parylene polymer layer can be performed during or after parylene monomer deposition. In addition, during a plasma treatment, a background pressure of a gas other than parylene monomer (i.e., a background gas) can be present. Preferably, the pressure of the background gas in the deposition chamber is from about 125 millitorr to about 375 millitorr, more preferably from about 200 millitorr to about 300 millitorr and most preferably from about 240 millitorr to about 260 millitorr. In some embodiments, a background gas is comprised of one or more noble gases. Examples of noble gases include helium, neon, argon and xenon. In other embodiments, a background gas can include one or more hydrocarbons. Such hydrocarbon background gases may be saturated hydrocarbons, unsaturated hydrocarbons, aromatic hydrocarbons, straight-chained hydrocarbons, branched hydrocarbons, cyclic hydrocarbons and the like. An exemplary list of hydrocarbons appropriate for use as background gases includes, but is not limited to, methane, ethane, ethylene and acetylene. In certain embodiments, a background gas can

comprise one or more noble gases and one or more hydrocarbon gases. It has been found that the use of one or more hydrocarbon gases results in parylene polymer layers having improved properties (see discussion below).

It is to be understood that the aforementioned treatments of parylene polymer layers may be performed on an entire parylene polymer layer or a portion of a parylene polymer layer. In addition, while certain treatments of parylene polymer layers have been disclosed herein, it is to be understood that other treatments of parylene polymer layers to enhance adhesion, or other properties, of these layers will be apparent to those skilled in the art and are intended to be within the scope of the present invention.

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Parylene polymers are usually highly crystalline and linear materials, which can limit the strength or other physical properties of these layers. To improve the strength of a parylene polymer layer, additional chemical species (e.g., monomers) other than parylene monomer, may be added to the layer during synthesis of the layer. When incorporated into the parylene polymer layer, these additional components should allow cross-linking to occur, increasing the strength and/or adhesion of the resulting layer. An illustrative and nonlimiting list of such chemical species includes species having a molecular formula C_xH_y where each of x and y is an integer of at least one.

Incorporation of these chemical species into a parylene polymer layer can be accomplished by, for example, establishing a background pressure of these other components within the deposition chamber during parylene monomer deposition. In certain embodiments, a pulsed plasma treatment or continuous plasma treatment can be used when a background pressure of one or more of these chemical species is present in the deposition chamber, but such pulsed plasma treatment or continuous plasma treatment is not required.

In embodiments of the present invention in which a chemical species other than parylene monomer is incorporated into a parylene polymer, the parylene polymer preferably should have an amount of the chemical species incorporated therein to improve the properties of the parylene polymer layer such that at least one of the advantages of the present invention as described herein is attained.

In some embodiments, enhanced adhesion may be achieved by providing a layer of adhesion promoting material between layer 16 and layer 14 and/or between layer 18 and layer 14.

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Alternatively, layer 16 and/or layer 18 may be formed from an adhesion promotion material.

Adhesion promotion materials appropriate for use in the present invention include, but are not limited to, organosilane compounds, metals, metal oxides and semiconductor oxides. Examples of such organosilane compounds include A-150 (available from Union Carbide Technologies), A-174 (available from Union Carbide Technologies) and VM 651 (available from DuPont Chemicals).

Other such adhesion promotion materials are known to those skilled in the art and are intended to be within the scope of the present invention. It is to be appreciated that, for these embodiments, layer 14 may or may not undergo any of the above-noted surface treatments.

For some applications, it may be advantageous to prevent the diffusion of materials through parylene polymer layer 14. For these applications, layer 16 and/or layer 18 may be formed from materials that reduce or eliminate the diffusion of materials through parylene polymer layer 14. Materials appropriate for use in these applications are disclosed in, for example, U.S. Patent No. 5,470,802. Other such materials are known to those skilled in the art and are intended to be within the scope of the present invention.

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For certain uses, such as, for example, electronic circuits, it may be desirable to form relatively flat layers, but, since parylene polymer layer 14 is comparatively conformal, layer 14 may not have the desired degree of flatness. Hence, it may be advantageous to grind or otherwise treat layer 14 to make it more flat, often referred as planarizing within the art. However, in certain embodiments, layer 14 may be difficult to planarize. For these embodiments, layer 16 and/or layer 18 may be formed from a material that is more readily planarized. Typically, such a material is a dielectric material, but, in some instances, it may be an electrical conductor.

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Fig. 4 shows a portion 30 of a multi-level electronic circuit according to the present invention. Portion 30 includes silicon wafer substrate 22, electrically insulating layer 24, electrically conductive layer 26, electrically conductive layer 28 and parylene polymer layer 14 disposed between layers 26 and 28.

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Silicon wafer substrate 22 may be formed from any of the standard substrate materials used in the electronics industry, such as, for example, a silicon backboard or a fiberglass backboard. Other appropriate structures for wafer substrate 22 are known to those skilled in the art and are intended to be within the scope of the present invention.

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Electrically insulating layer 24 typically functions to protect wafer substrate 22 from electrically conductive layers 26 and 28. Layer 24 is usually formed from silicon dioxide, although other appropriate materials may be used. Electrically insulating layer 24 may be formed according to any of the standard techniques known to those skilled in the art.

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Electrically conductive layers 26 and 28 may be formed from metals or other materials appropriate for use in electronic circuits. Layers 26 and 28 may comprise metal conductor lines which are formed according to standard photolithographic and etching techniques. For such embodiments, layers 26 and 28 may each correspond to a power plane, a ground plane or an interconnection trace layer.

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Electrically conductive layers 26 and 28 may be interconnected through parylene polymer layer 14 by use of vias, or through holes (not shown), which are formed in parylene polymer layer 14 by conventional processes known to those skilled in the art.

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According to the present invention, parylene polymer layer 14 is formed using a vapor deposition process. Preferably, the vapor deposition process allows the monomer to be formed outside the deposition portion of the vacuum chamber such that the monomers can undergo a purification process prior to being deposited onto the substrate. In a particularly preferred embodiment, parylene polymer layer 14 is formed using a vacuum chamber 40 as depicted in Fig. 5. Vacuum chamber 40 includes vaporization zone 42, a pyrolysis zone 44, a post-pyrolysis zone 46 and a deposition zone 48. Examples of such vacuum chamber are disclosed in, for example, commonly assigned U.S. Patent No. 5,546,473, which is herein incorporated by reference.

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A dimer material having the structure:

is placed within vaporization zone 42 at about room temperature and subsequently heated to a temperature of from about 70°C to about 150°C to vaporize the dimer.

The vaporized dimer passes into pyrolysis zone 44 which is maintained at a temperature of from about 600°C to about 720°C to pyrolize the dimer (i.e., cleave certain chemical bonds) and form a monomer having the following structure:

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The monomer passes through post-pyrolysis zone 46 which is maintained at a temperature of at most about room temperature. At this temperature, residual vaporized dimer can adhere to the walls of post-pyrolysis zone 46 while the monomer generally passes through post-pyrolysis zone 46 without adhering to the walls of zone 46. Thus, post-pyrolysis zone 46 reduces the amount of vaporized dimer that ultimately enter deposition chamber 48. In certain embodiments, this feature can be advantageous because the vaporized dimer can constitute an impurity in parylene polymer layer 14, which may have an undesirable local effect on the dielectric constant or other properties of layer 14.

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After passing through post-pyrolysis zone 46, the monomer enters deposition chamber 48 which includes substrate 50. Substrate 50 is placed on a platen 52 that includes a standard temperature controlling device 54 that controls the temperature by the platen by heating and/or cooling platen 54. By use of device 54, the temperature of substrate 50 and platen 52 is typically held at a temperature of from about room temperature to about -25°C during deposition of the monomer onto substrate 50.

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It has been found that reducing the temperature of substrate 50 and platen 52 during monomer deposition can provide several advantages, including more control of the overall process of making parylene polymer layer 14 by allowing for increased manipulation of the monomer. For example, cooling substrate 50 and platen 52 allows for the walls of deposition chamber 48 to be

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heated during monomer deposition. In addition, reducing the temperature of substrate 50 and platen 52 during monomer deposition results in a more efficient deposition process and a more efficient use of the parylene dimer starting material.

Subsequent to monomer deposition, device 54 may be used to increase the temperature of substrate 50 and platen 52 to a temperature of from about 100°C to about 400°C to anneal the parylene polymer layer. However, it is to be noted that polymerization of the parylene monomer occurs spontaneously at the temperatures of substrate 50 noted above.

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Prior to placing the dimer within vaporization zone 46, the dimer is first purified. Since the dimer of the present invention has a high degree of symmetry, it is readily purified by crystallization. Typically, these solvents are relatively unsymmetric in order to have a high temperature coefficient of solubility. However, if the solvent is too symmetric, separation of the solvent from the dimer may be difficult. Without wishing to be bound by any theories, it is believed that this increased difficulty in solvent/dimer separation results from the accidental accommodation of the solvent within the dimer lattice. Solvents appropriate for use in dimer crystallization according to the present invention include, but are not limited to, chloroform, tetrahydrofuran, methylene chloride, and linear hydrocarbons such as n-hexane and n-heptane. In a preferred embodiment, the solvent is n-hexane. After dissolving the dimer in the solvent, this solution is typically passed through a chromatographic bed including a polar material such as, for example, alumina. The polar nature of the chromatographic bed removes many of the polar or ionic impurities present within the solution. Furthermore, the chromatographic bed can remove fine impurities within the solution by filtration.

Using this process has been found to produce parylene polymer layers which have reduced levels of impurities. For example, parylene polymer layers in accordance with the present invention may have zinc impurity levels of 66 parts per billion or less. This feature of the present invention is desirable because impurities within parylene polymers can result in several different negative effects, including, but not limited to, an increase in the dielectric constant of the parylene polymer layer, a decrease in the surface resistivity of the parylene polymer layer and/or electron storm formation within the multi-level structure.

While particular apparatuses and methods of making parylene polymer layer 14 have been

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described herein, one skilled in the art would understand that at least certain aspects of these apparatuses and methods may be varied or modified, and such variations and modifications are intended to be within the scope of the present invention. For example, in addition to cleaving the parylene dimer bond by use of elevated temperature as discussed above, the parylene dimer may be cleaved by use of a plasma. Such methods are disclosed in, for example, Russian Patent Nos. RU 2,000,850 and RU 2,002,519.

When used in integrated circuits or for other electronics applications, parylene polymer layer 14 should have a minimal dielectric constant to enhance circuit operating speed and decrease power consumption. Accordingly, these parylene polymer layers preferably have a dielectric constant of at most about 2.6, more preferably at most about 2.4 and most preferably at most about 2.2.

Having a low dissipation factor decreases the signal loss in an integrated circuit. Therefore, parylene polymer layers in accordance with the present invention preferably have a dissipation factor of less than about 0.001.

According to the present invention, parylene polymer layers with a thickness of about one micrometer preferably have a breakdown voltage of at least about 750 volts.

Parylene polymer layer 14 preferably has a Young's modulus of about 5 gigapascals.

The elongation to break of parylene polymer layers according to the present invention is preferably at least about 20%.

Parylene polymer layer 14 preferably has an ultimate tensile strength of at least about 122 megapascals.

According to the present invention, parylene polymer layers have water absorption values of at most about 0.5% by weight, more preferably at most about 0.2% by weight and most preferably at most about 0.1% by weight.

Parylene polymer layers in accordance with the present invention preferably have a thermal stability such that these layers demonstrate less than 1% weight loss per 2 hours at a temperature of at least about 450°C.

Parylene polymer layer 14 preferably has a crystalline melting point of above about 500°C.

The surface resistivity of parylene polymer layers in accordance with the present invention is preferably about 1.3x10¹⁴ ohms.

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The volume resistivity of parylene polymer layer 14 is preferably about 5.3x10¹⁶ ohms.

Parylene polymer layers in accordance with the present invention preferably have a density of about 1.58.

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The thermal expansion at 25°C of parylene polymer layer 14 is preferably at most about 35 parts per million.

According to the present invention, parylene polymer layers have a coefficient of friction of about 0.2.

The following are illustrative examples of embodiments of the present invention. They are not to be construed as limiting.

10 Example 1

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The following process was performed in a jacketed Soxhlet extractor (available as catalog number LG-6950, from Lab Glass, located in Vineland, NJ or as catalog number CG-1328, available from Chem Glass, located in Vineland, NJ). An amount of the crude dimer used as the starting material in the synthesis of the parylene polymer layers of the present invention was placed within a glass extraction thimble with a fritted glass disk at its bottom. A short chromatographic bed of particulate alumina was placed at the bottom of the thimble. The thimble was purchased with a diameter of 41 mm and a height of 130 mm. The height of the thimble was increased to 180 mm to accommodate larger samples (i.e., up to about 70 grams) of the crude dimer.

A flask of boiling n-hexane was placed below the thimble, and gaseous n-hexane was condensed in a condenser mounted above the thimble. The condensed n-hexane dripped onto the crude dimer to form a leachant solution of the condensed n-hexane, purified dimer and impurities, including dirt, dust, and/or polymers or oligomers of the monomer formed by the dimer. The leachant solution passed through the chromatographic bed and fritted glass at the bottom of the thimble. The chromatographic bed removed many polar or ionic impurities present within the leachant solution due to the polar nature of alumina. In addition, the chromatographic bed removed fine impurities by filtration.

A siphoning mechanism was used to periodically empty the leachant solution from the Soxhlet extractor holding the thimble. This process returned the n-hexane from the leachant solution to the flask of boiling n-hexane. After a period of from about 10 to about 20 hours, the

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crude dimer ended up in the flask of boiling n-hexane.

The extraction was conducted at the boiling n-hexane to speed up the dimer dissolution process. To accomplish this, a conduit jacket surrounded the extraction volume, so the extraction volume was heated by vapors of n-hexane as these vapors traveled from the boiling flask to the condenser. While this hot filtration process is advantageous because impurities are removed while the solution is hot, it is to be noted that, in conventional crystallization equipment, such a hot filtration can be difficult and/or dangerous when flammable solvents are used. Furthermore, for practical reasons, such a filtration may be performed at temperatures below the solvent boiling temperature, resulting in increased solvent use and decreased dimer solubility. However, using a Soxhlet apparatus, the boiling solvent vapors are held within the apparatus by the jacket, allowing for increased efficiency in the purification process.

The resulting purified dimer of the present invention was tested by inductively coupled plasma-mass spectrometry of the vaporized dimer. During this process, the sample is ashed to remove carbon containing components, leaving nonvolatile oxides of the trace elements to be determined. This ash is taken up in an aqueous buffer solution. The aqueous buffer solution of the sample ash is fed to an energized plasma. The high temperature of the plasma atomizes the trace elements. The atomized plasma is fed to the source of a mass spectrometer for quantification of each specific impurity elements.

The results are shown in Table 1, which clearly demonstrates that the zinc impurity levels are about 66 parts per billion. This method does not involve a direct measurement of the impurity level of the parylene polymer layer formed from the monomers. However, by measuring the impurity level of the starting material (i.e., dimer) for parylene polymer film synthesis, this method does provide an upper limit on the possible impurity level of the parylene polymer films of the present invention.

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Table 1

Element	Impurity Level
	(Parts per Billion)
Al	460

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	Ва	6.2
	Ве	<10
	Bi	<10
	Cd	<12
5	Ca	660
	Cs	880
	Cr	10
	Со	<1
	Cu	<5
10	Ga	<1
	In	<1
	Fe	140
	Pb	7.4
	Li	37
15	Mg	83
	Mn	2.3
	Мо	<5
	Ni	7.8
	К	99
20	Rb	<1
	Ag	<10
	Na	500
	Sr	<1
	Th	<10
25	Sn	310
	V	<1
	Zn	66

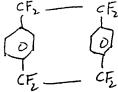
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Zr	<10
L	<u></u>

To purify about 70 grams of crude dimer according to this process, about 3 liters of n-hexane may be used. In this embodiment of the process, a 1 liter flask having an initial volume of about 0.7 l of n-hexane is utilized.

Example 2

A parylene polymer layer was formed was formed without a pulsed plasma treatment as follows. The deposition apparatus was as described in U.S. Patent No. 5,546,473. 0.5 grams of parylene dimer were placed into a crucible within the vaporization zone. The parylene dimer had the molecular structure:



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The crucible was heated to 105°C for thirty minutes, and the dimer was vaporized. The vaporized dimer passed into the pyrolysis zone which was held at 640°C. The dimer was pyrolized to form parylene monomer in the pyrolysis zone, and the parylene monomer was passed through the post-pyrolysis zone which was held at -100°C. Parylene monomer deposited on the surface of a six inch silicon wafer which was attached to a platen held at -15°C. The resulting parylene polymer layer had a thickness of 1 micrometer, and the deposition rate was 700Å per minute.

Example 3

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A parylene polymer layer was formed using the method described in Example 2, but a pulsed plasma treatment was used during the parylene monomer deposition. The resulting parylene polymer layer had a thickness of 3 micrometers, and the deposition rate was 2100Å per minute.

Having thus described particular embodiments of the present invention, various alterations, modifications and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements are intended to be part of this disclosure, and are intended to be

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within the spirit and scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended as limited. The present invention is limited only as defined by the following claims and the equivalents thereto.

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CLAIMS

1. A method of forming a parylene polymer layer, the method comprising the steps of: depositing monomers of parylene onto a surface of a substrate to form a layer; and treating the layer with a pulsed plasma treatment.

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- 2. The method according to claim 1, wherein the depositing step and the treating step are performed simultaneously.
- The method according to claim 1, wherein the treating step is performed after the depositingstep.
 - 4. The method according to claim 1, further comprising the step of: establishing a pressure of a background gas sufficient to allow deposition of the background gas onto the surface of the substrate.

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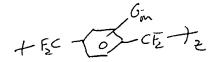
- 5. The method according to claim 4, wherein the establishing step is performed simultaneously with the depositing step.
- 6. The method according to claim 4, wherein the pressure of the background gas is from about 125 millitorr to about 375 millitorr.
 - 7. The method according to claim 4, wherein the background gas is a hydrocarbon.
 - 8. The method according to claim 4, wherein the background gas is selected from the group consisting of methane, ethane, ethane, acetylene, and combinations thereof.
 - 9. The method according to claim 1, wherein the treating step includes using a duty cycle of from about 0.1% to about 50%.

- 10. The method according to claim 1, wherein the treating step includes using a duty cycle of from about 0.2% to about 10%.
- 11. The method according to claim 1, wherein the treating step includes using a duty cycle of from about 0.2%.
 - 12. The method according to claim 1, wherein the treating step includes using a peak power of from about 0.05 Watts/inch³ to about 100 Watts/inch³.
- 10 13. The method according to claim 1, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 20 Watts/inch³.
 - 14. The method according to claim 1, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 10 Watts/inch³.

15. A multi-level structure, comprising:

a first layer having a surface; and

a parylene polymer layer having first and second surfaces, the first surface of the parylene polymer layer being opposite to the second surface of the parylene polymer layer, the first surface of the parylene polymer layer being disposed along the surface of the first layer, the parylene polymer layer being formed from a material having a structure:



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wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most

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equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 66 parts per billion; and

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a layer of adhesion promoting material having a first surface and a second surface, the first surface of the layer of adhesion material being disposed along the second surface of the parylene polymer layer.

- 16. The multi-level structure according to claim 15, wherein the adhesion promoting material is an organosilane.
- 10 17. The multi-level structure according to claim 15, wherein the adhesion promoting material is selected from the group consisting of organosilane compounds, metals, metal oxides and silicon oxides.
- 18. The multi-level structure according to claim 15, wherein the adhesion promoting material is selected from the group consisting of metals, metal oxides and semiconductor oxides.
 - 19. The multi-level structure according to claim 15, further comprising a second layer having a surface, wherein the second layer of the adhesion material is disposed along the surface of the second layer such that the parylene polymer layer is disposed between the first and second layers.
 - 20. The multi-level structure according to claim 19, wherein the first layer is an electrically conductive material.
- 21. The multi-level structure according to claim 20, wherein the second layer is formed from an electrically conductive material.
 - 22. The multi-level structure according to claim 15, wherein the parylene polymer layer has a dielectric constant of at most about 2.6.

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- 23. The multi-level structure according to claim 15, wherein the parylene polymer layer has a zinc impurity level of about 66 parts per billion.
- 24. A method making a multi-level structure, comprising the steps of:

 depositing a monomer on a surface of a substrate to form a layer; and

 treating the layer with a pulsed plasma treatment to form a parylene polymer film on the

 surface of the first layer, the parylene polymer having a structure:

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wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 66 parts per billion.

- 25. The method according to claim 24, further comprising the steps of: vaporizing a parylene dimer; and pyrolyzing the parylene dimer to form the monomer.
- 26. The method according to claim 25, wherein the depositing step occurs in a deposition zone of a vacuum chamber.
- 25 27. The method according to claim 26, wherein the pyrolyzing step occurs outside the deposition zone of the vacuum chamber.
 - 28. The method according to claim 27, further comprising the step of feeding the monomer into the deposition zone of the vacuum chamber.

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- 29. The method according to claim 27, wherein the polymerizing step includes polymerizing the monomer to form a parylene polymer film having a zinc impurity level of about 66 parts per billion.
- 30. The method according to claim 24, wherein the depositing step and the treating step areperformed simultaneously.
 - 31. The method according to claim 24, wherein the treating step is performed after the depositing step.
- The method according to claim 24, further comprising the step of:
 establishing a pressure of a background gas sufficient to allow deposition of the background
 gas onto the surface of the substrate.
 - 33. The method according to claim 32, wherein the establishing step is performed simultaneously with the depositing step.

- 34. The method according to claim 32, wherein the pressure of the background gas is from about 125 millitorr to about 375 millitorr.
- The method according to claim 32, wherein the background gas is a hydrocarbon.
 - 36. The method according to claim 32, wherein the background gas is selected from the group consisting of methane, ethane, ethylene, acetylene, and combinations thereof.
- 25 37. The method according to claim 24, wherein the treating step includes using a duty cycle of from about 0.1% to about 50%.
 - 38. The method according to claim 24, wherein the treating step includes using a duty cycle of from about 0.2% to about 10%.

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- 39. The method according to claim 24, wherein the treating step includes using a duty cycle of from about 0.2%.
- 40. The method according to claim 24, wherein the treating step includes using a peak power of from about 0.05 Watts/inch³ to about 100 Watts/inch³.
 - 41. The method according to claim 24, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 20 Watts/inch³.
- 10 42. The method according to claim 24, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 10 Watts/inch³.
 - 43. A multi-level structure, comprising:
 - a first layer having a surface; and
- a parylene polymer layer disposed along the surface of the first layer, the parylene polymer layer being formed from a material having a structure:



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wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero, and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 66 parts per billion and wherein the parylene polymer layer is formed by a process including the steps of:

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depositing monomers of parylene onto a surface of a substrate to form a layer; and treating the layer with a pulsed plasma treatment.

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- 5 44. The multi-level according to claim 43, wherein the depositing step and the treating step are performed simultaneously.
 - 45. The multi-level according to claim 43, wherein the treating step is performed after the depositing step.
 - 46. The multi-level according to claim 43, further comprising the step of:
 establishing a pressure of a background gas sufficient to allow deposition of the background
 gas onto the surface of the substrate.
- 15 47. The multi-level according to claim 46, wherein the establishing step is performed simultaneously with the depositing step.
 - 48. The multi-level according to claim 46, wherein the pressure of the background gas is from 125 millitorr to about 375 millitorr.
 - 49. The multi-level according to claim 46, wherein the background gas is a hydrocarbon.
 - 50. The multi-level according to claim 46, wherein the background gas is selected from the group consisting of methane, ethane, ethylene, acetylene, and combinations thereof.
 - 51. The multi-level according to claim 43, wherein the treating step includes using a duty cycle of from about 0.1% to about 50%.
 - 52. The multi-level according to claim 43, wherein the treating step includes using a duty cycle

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of from about 0.2% to about 10%.

53. The multi-level according to claim 43, wherein the treating step includes using a duty cycle of from about 0.2%.

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- 54. The multi-level according to claim 43, wherein the treating step includes using a peak power of from about 0.05 Watts/inch³ to about 100 Watts/inch³.
- The multi-level according to claim 43, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 20 Watts/inch³.
 - 56. The multi-level according to claim 43, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 10 Watts/inch³.
- 15 57. A multi-level structure, comprising:
 - a first layer having a surface; and
 - a parylene polymer layer disposed along the surface of the first layer, wherein the parylene polymer is formed by a process including the steps of:
 - depositing monomers of parylene onto a surface of a substrate to form a layer; and treating the layer with a pulsed plasma treatment.
 - 58. The multi-level according to claim 57, wherein the depositing step and the treating step are performed simultaneously.
- 25 59. The multi-level according to claim 57, wherein the treating step is performed after the depositing step.
 - 60. The multi-level according to claim 57, further comprising the step of:
 establishing a pressure of a background gas sufficient to allow deposition of the background

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gas onto the surface of the substrate.

61. The multi-level according to claim 60, wherein the establishing step is performed simultaneously with the depositing step.

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- 62. The multi-level according to claim 60, wherein the pressure of the background gas is from about 125 millitorr to about 375 millitorr.
- 63. The multi-level according to claim 60, wherein the background gas is a hydrocarbon.

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- 64. The multi-level according to claim 60, wherein the background gas is selected from the group consisting of methane, ethane, ethylene, acetylene, and combinations thereof.
- 65. The multi-level according to claim 57, wherein the treating step includes using a duty cycle of from about 0.1% to about 50%.
 - 66. The multi-level according to claim 57, wherein the treating step includes using a duty cycle of from about 0.2% to about 10%.
- 20 67. The multi-level according to claim 57, wherein the treating step includes using a duty cycle of from about 0.2%.
 - 68. The multi-level according to claim 57, wherein the treating step includes using a peak power of from about 0.05 Watts/inch³ to about 100 Watts/inch³.

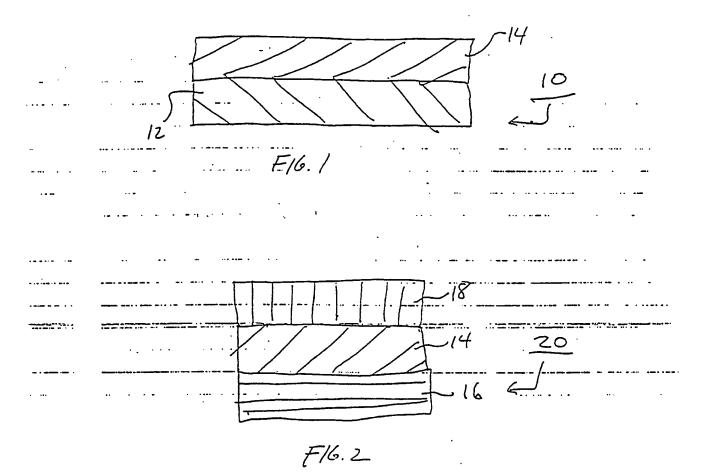
- 69. The multi-level according to claim 57, wherein the treating step includes using a peak power of from about 0.1 Watts/inch³ to about 20 Watts/inch³.
- 70. The multi-level according to claim 57, wherein the treating step includes using a peak power

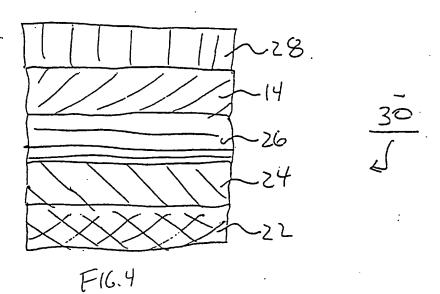
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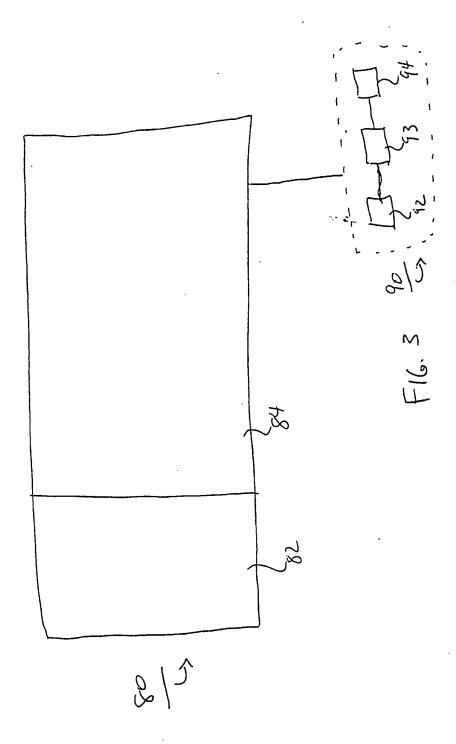
of from about 0.1 Watts/inch3 to about 10 Watts/inch3.

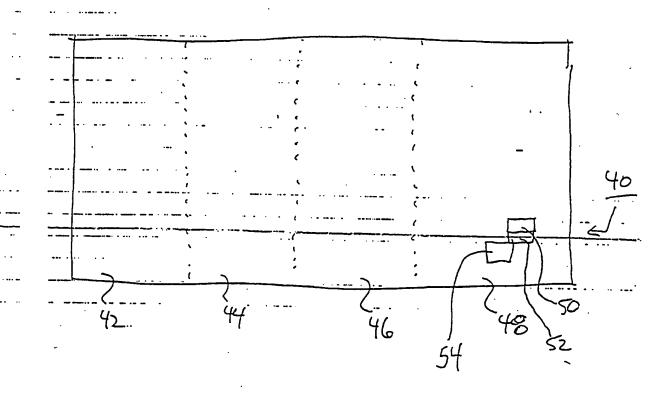
71. The multi-level structure according to claim 15, wherein the parylene polymer layer further includes a chemical species other than parylene monomer.

- 72. The multi-level structure according to claim 43, wherein the parylene polymer layer further includes a chemical species other than parylene monomer.
- 73. The multi-level structure according to claim 57, wherein the parylene polymer layer further includes a chemical species other than parylene monomer.









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Int .tional Application No PCT/US 97/19294

A. CLASSI IPC 6	ification of subject matter B05D7/24 B05D3/14		
	o International Patent Classification(IPC) or to both national classifica	tion and IPC	
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C. DOCUM	ENTS CONSIDERED TO BE RELEVANT		
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X Furt	her documents are listed in the continuation of box C.	X Patent family members are listed in	annex.
* Special ca	stegories of cited documents :	"T" later document published after the intern	
consid	ent defining the general state of the art which is not dered to be of particular relevance document but published on or after the international	or priority date and not in conflict with the cited to understand the principle or the invention	ory underlying the
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Name and	mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NI - 2280 AV Bitadily	Authorized officer	
	NL - 2260 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Brothier, J-A	

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